Syllabus of Record

Program: CET Siena
Course Code / Title: (SN/CS3330) Computer Architecture
Total Hours: 45
Recommended Credits: 3
Primary Discipline / Suggested Cross Listings: Computer Science / Data Science
Language of Instruction: English
Prerequisites / Requirements: UVA students: CS2150 Program and Data Representation. Equivalent courses for students from another institution

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Description
This course provides students with a solid understanding of fundamental architectural techniques used to build today's high-performance processors and systems. This course is structured with a 35% lab component and 65% in-class teaching.

Objectives
Through their participation in this course, students:

- Learn how to choose a computer by examining the parameters that influence its performance.
- Analyze the effectiveness of the architectural mechanisms to improve the capabilities of computers.
- Learn how to analyze and design combinational and sequential digital systems.
- Identify the structure of the main logical components at the base of digital circuits (e.g., registers, decoders, mux, counters).
- Master how to design a system composed of digital circuits.
- Learn the architectural elements of a modern computer and of the structure of the processor, Memory Subsystem and Input/Output Subsystem.

Course Requirements
Active participation is essential in this course. Students are expected to attend each class and lab session, as outlined in the CET Attendance Policy. Students are expected to read all assigned materials and complete homework before each class session. Reading assignments are generally 20-30 pages per class session. Graded assignments include:

- Homework/Lab: weekly assignments.
- Final Exam: a written test taken in the laboratory, where the simulator can be used for assembly language and for Verilog language for immediate verification of the exercises.
- Oral Exam: consists of questions on topics covered during the lectures.

Grading

The final grade is determined as follows:

- Participation: 20%
- Homework/Lab: 40%
- Final Exam: 20%
- Oral Exam: 20%

Readings

Patterson, David and John Hennessy. *Computer Organization and Design RISC-V Edition: The Hardware Software Interface*. Waltham, MA: Morgan Kaufman/Elsevier, 2017.

Heuring, Vincent. *Computer Systems Design and Architecture, Second Edition.* London: Pearson, 2003.

Stallings, William. *Computer Organization and Architecture*. London: Pearson, 2015.

Tanenbaum, Andrew. *Structured Computer Organization, Fourth Edition*. New Jersey: Prentice Hall, 1998.

Outline of Course Content

Every topic addressed in class is supplemented by lab sessions. Two to three weeks is spent on each of the below areas.

Topic 1: Digital Systems Elements of Design

- CMOS technology: NOT, NAND, NOR ports, transit port (stick diagram and CMOS circuit)
- Propagation delays, output input characteristics, noise margins and their dependence on physical parameters.
- Boolean algebra. Standard forms of Boolean functions and Karnaugh maps.
- Decoder, Encoder, Priority Encoder, Multiplexer, Demultiplexer, Look-Up-Table (LUT), Half-Adder, Full-Adder, ALU.
- Verilog and creation of a simple processor with RISC-V architecture.
- SR latches and flip-flops, clocked-SR, SR-master-salve, D-latch, D-edge-triggered and their transistor-level realizations.
- Two-phase clock generation.
- Mealy and Moore machines: VERILOG models and classical synthesis.
- Flip-Flop JK and T.
- Counters: Ripple, Serial Carry, Parallel Carry, Ring Counter.
- Parallel adder with serial carry-over and look-ahead report.

Topic 2: Machine Organization and Assembly

- Principles of RISC-V microprocessors.
- Instructions formats and basic instructions.
- Assembly: addressing mode. Function call. Performance equation. Performance evaluation, SPEC benchmark set. Amdahl's law.

- Two-pass assembler
- Loading, connecting multiple modules.
- IEEE-754 standard for floating-point.
- Floating-point registers and instructions in the processor.
- Exceptions and interrupts. Interrupt management routine. Precise and inaccurate interrupts.

Topic 3: Memory Subsystem

- Types of memory. Difference between SRAM and DRAM. Reading and writing cycle in DRAM. Memory Hierarchy and Locality Principle.
- Cache architecture: direct access cache. Parameters characterizing the functioning of the caches. Associative Cache. Multi-level cache. Dependency of a computer's performance on the cache.
- Virtual Memory: hardware mechanisms to support it.
- Paging with 2 or more levels and with a reverse table.
- TLB: Translation Lookaside Buffer.

Topic 4: I / O and Communications

- Types of buses.
- Synchronous and asynchronous exchange protocol. Arbitrage (master / slave, daisy-chain).
- Overview of PCI buses.
- Drive devices: polling, interrupt, DMA techniques.
- The case of PCs: interrupt controller 8259A.
- Internal complexity of the chips: timer 8254, UART 16550A.
- Communications on serial buses (packaging, Ethernet, USB).

Topic 5: Processor

- Processors with pipelines.
- Resolving pipeline conflicts.
- Limits of the pipeline and outline of superscalar processors.